FIG. 1

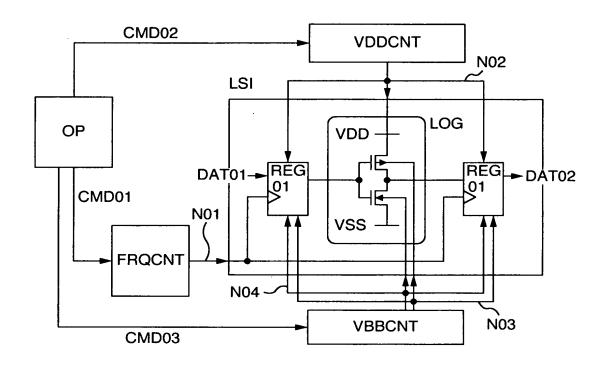
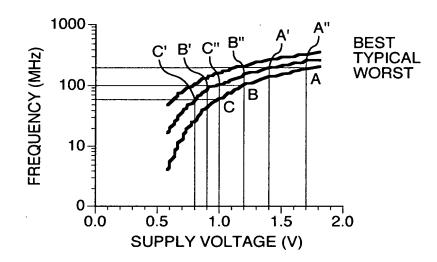


FIG. 2

FRQ	VDD (WITHOUT VBB)	VDD (WITH VBB)
200 MHz	1.7V	1.4V
100 MHz	1.2V	0.9V
50 MHz	1.0V	0.8V

FIG. 3



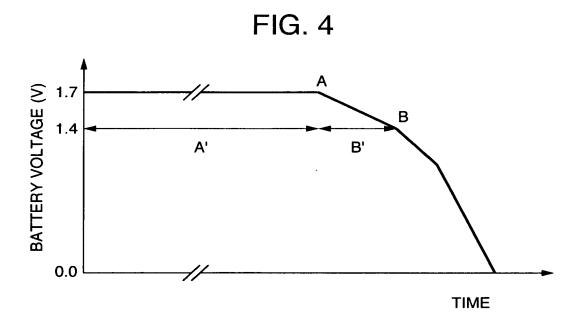


FIG. 5

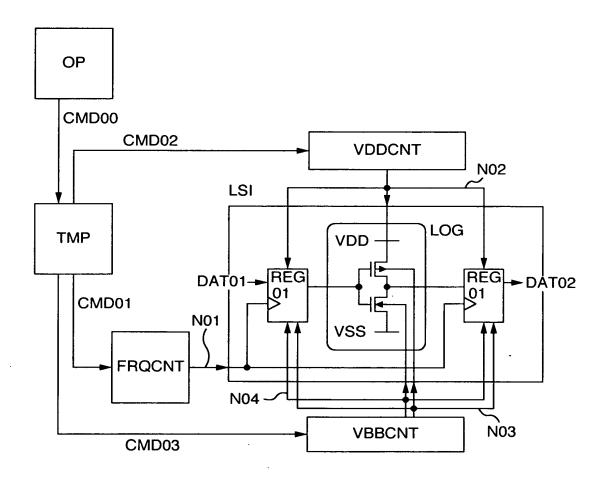


FIG. 6

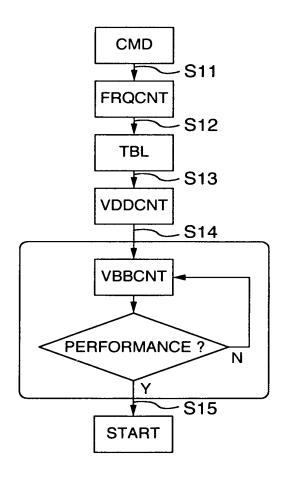


FIG. 7

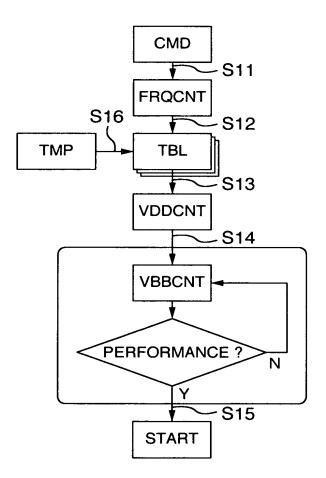


FIG. 8

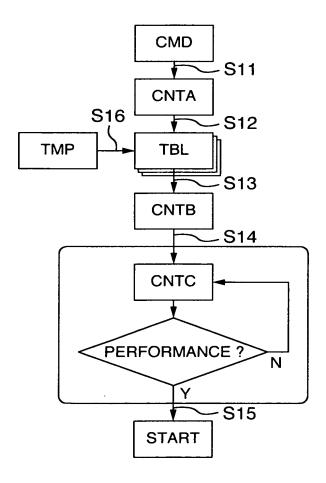


FIG. 9

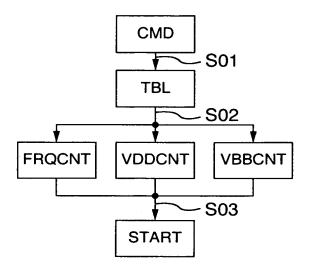


FIG. 10

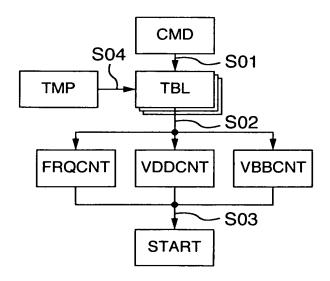


FIG. 11

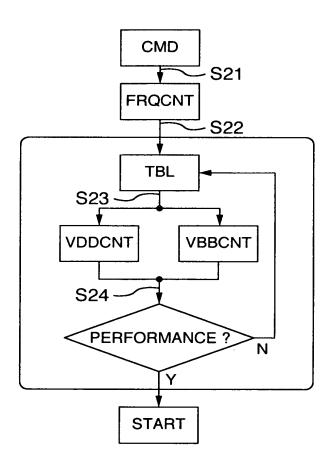


FIG. 12

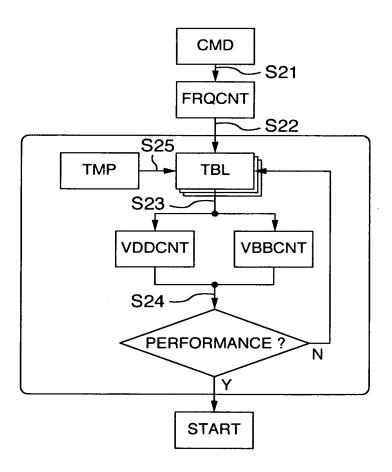


FIG. 13

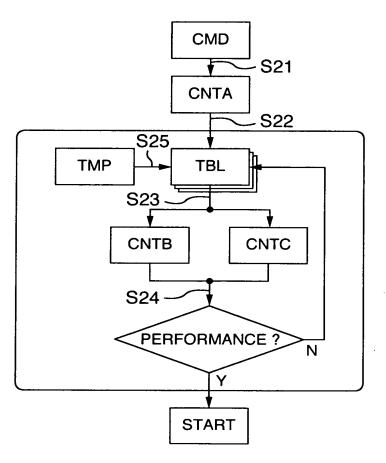


FIG. 14

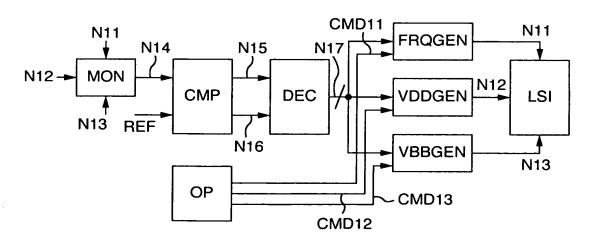


FIG. 15

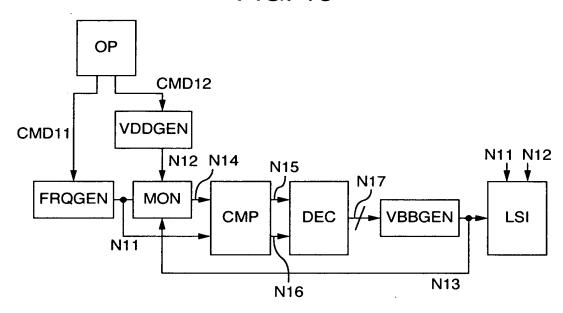


FIG. 16 N12 N11 N13 N14 N15 N17 FRQGEN MON CMP DEC **VDDGEN** LSI N11 N13 N16 CMD11 VBBGEN OP CMD13

FIG. 17

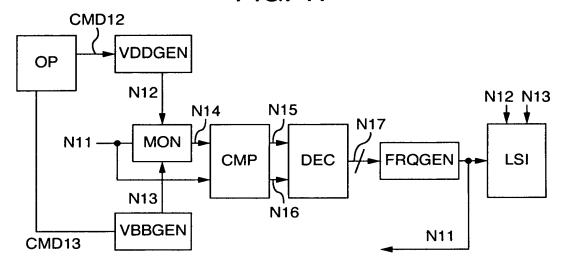


FIG. 18

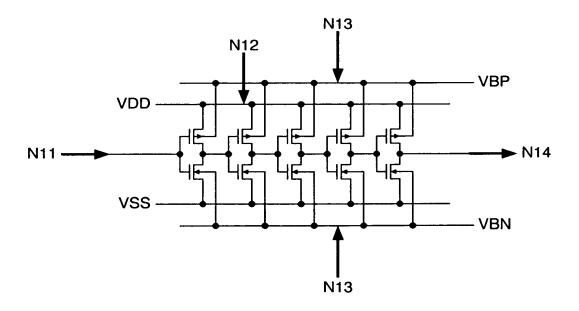


FIG. 19

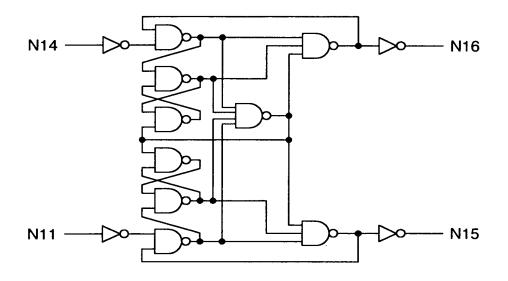


FIG. 20

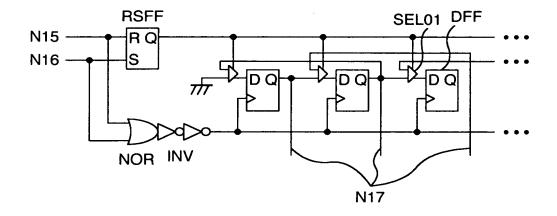


FIG. 21

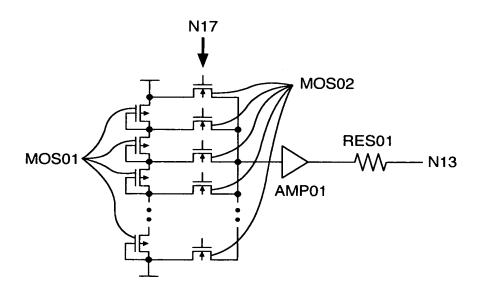


FIG. 22

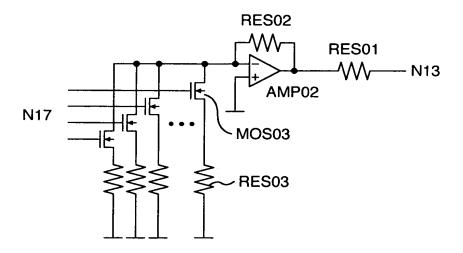


FIG. 23

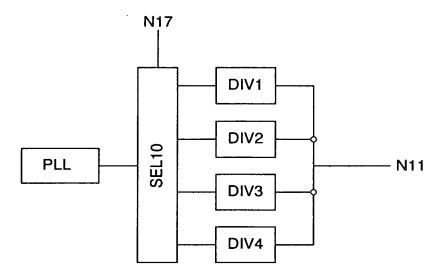


FIG. 24

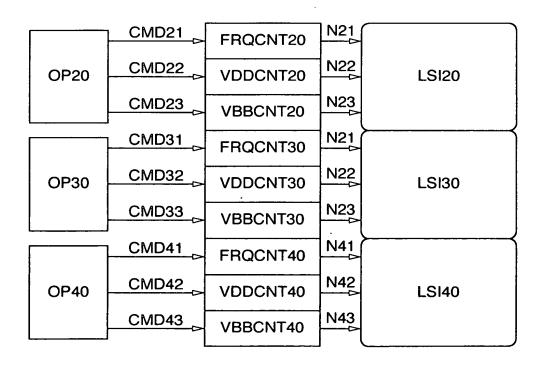


FIG. 25

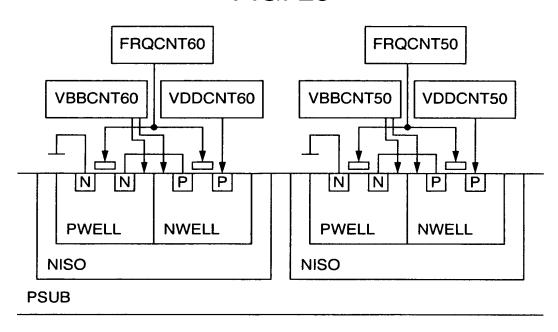


FIG. 26

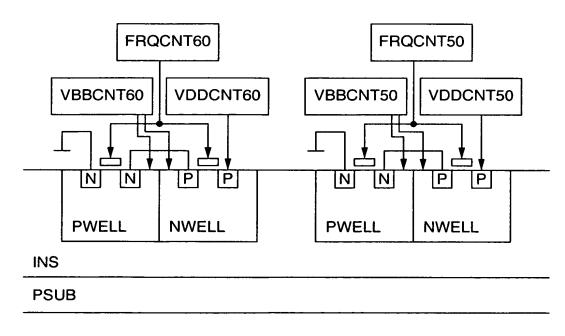


FIG. 27

